MHCG8D5-DNC-8VT1

Features

- Hot-pluggable OSFP form factor
- Support 800Gbps aggregate bit rates
- Up to 106.25Gbps Data rate per channel
- Maximum link length of 500m on Singalmode Fiber (SMF)
- Dual MPO-12 APC connector receptacle
- Case temperature range(not environment): 0 ~ +70℃
- Power dissipation: <18W
- Single 3.3V power supply

Application

- Data center
- 800GBASE-DR8 Ethernet

Standard

- Compliant to OSFP MSA
- Compliant with IEEE 802.3ck
- RoHS complaint

1. General Description

MHCG8D5-DNC-8VT1 is designed to transmit and receive serial optical data links up to 106.25 Gbps data rate (per channel) by PAM4 modulation format over single-mode fiber. It is a small-form- factor RHS hot pluggable transceiver module base on high performance SIP modulator. It is compliant with 800G Ethernet, OSFP MSA.

2. Absolute Maximum Ratings

It has to be noted that the operation in of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	+85	°C
Operating Humidity	RH	5	85	%
Supply Voltage	Vcc	-0.4	3.6	V

3. Recommended Operating Environment

Recommended Operating Environment specifies parameters for which the electrical and optical characteristics hold unless otherwise noted.

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		+70	°C
Supply Voltage	Vcc	3.135	3.3	3.465	V
Supply Current	Icc			5.15	A
Bit Rate	BR	800.00			Gbps
Fiber Length on OM3 SMF				500	m

4. Optical Characteristics

The following Optical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Optical Characteristics						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**NOTE**
Transiver						
Modulation format			PAM4			
Signaling rate, each lane (range)			53.125±100ppm		GBd	
Center Wavelength	λ0	1304.5		1317.5	nm	
Spectral Width (RMS)	σ			0.6	nm	1
Average Launch Power,each lane		-2.9		4	dBm	
Outer Optical Modulation Amplitude (OMAouter), each lane (max)				4.2	dBm	
Outer Optical Modulation Amplitude (OMAouter), each lane (min)		-0.8				2
Launch power in OMA_{outer} minus TDECQ (min)		-2.2			dBm	
Transmitter and dispersion eye closure (TDECQ), each lane (max)	TDECQ			3.4	dBm	
Average launch power of OFF transmitter, each lane (max)				-15	dBm	
Extinction Ratio, each lane	ER	3.5			dB	
Optical Return Loss Tolerance	ORL			21.4	dB	
Receiver						
Signaling rate, each lane (range)			53.125±100ppm		GBd	
Modulation format			PAM4			
Receiver Wavelength	λ	1304.5		1317.5	nm	
Damage threshold(min)		5			dBm	3
Average receive power, each lane (max)				4	dBm	
Average receive power, each lane (min)		-5.9			dBm	4
Receive power, each lane (OMAouter) (max)				4.2	dBm	
Receiver Reflectance	Rr			-26	dB	
Stressed receiver sensitivity (OMA)， each lane	Rsens			-1.9	dBm	
Receiver sensitivity (OMA outer), each lane (max)			RS = max (-3.9 , SECQ – 5.3)		dB	

Conditions of stressed receiver sensitivity test:						
Stressed eye closure for PAM4 (SECQ), lane under test			3.4		dB	6
OMA outer of each aggressor lane			4.2		dBm	6

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. Even if the TDECQ < 1.4dB, the OMA (min) must exceed this value.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.
6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

5. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	NOTE
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Current	Icc			5500	mA	
Transmitter						
Input differential impedance	Rin		100		Ω	1
Differential data input swing	Vin,pp	400		900	mV	
Receiver						
Differential data output swing	Vout,pp			900	mV	2

Notes:

1. Connected directly to TX data input pins.
2. In to 100Ω differential termination.

6. Digital Diagnostic Monitoring Information

Parameter	Accuracy	Calibration	Note
Temperature	±3°C	Internal	
Voltage	±3%	Internal	
Bias Current	±10%	Internal	
TX Power	±3dB	Internal	
RX Power	±3dB	Internal	

7. Pin Assignment

The OSFP modules are hot-pluggable. Hot pluggable refers to plugging in or unplugging a module while the host board is powered. The module contacts mates with the host in the order of ground, power, followed by signal as illustrated by Figure 1 and the contact sequence order listed in Table 1

Figure1 OSFP Pin Assignment

Table 1 OSFP connector pin list

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	

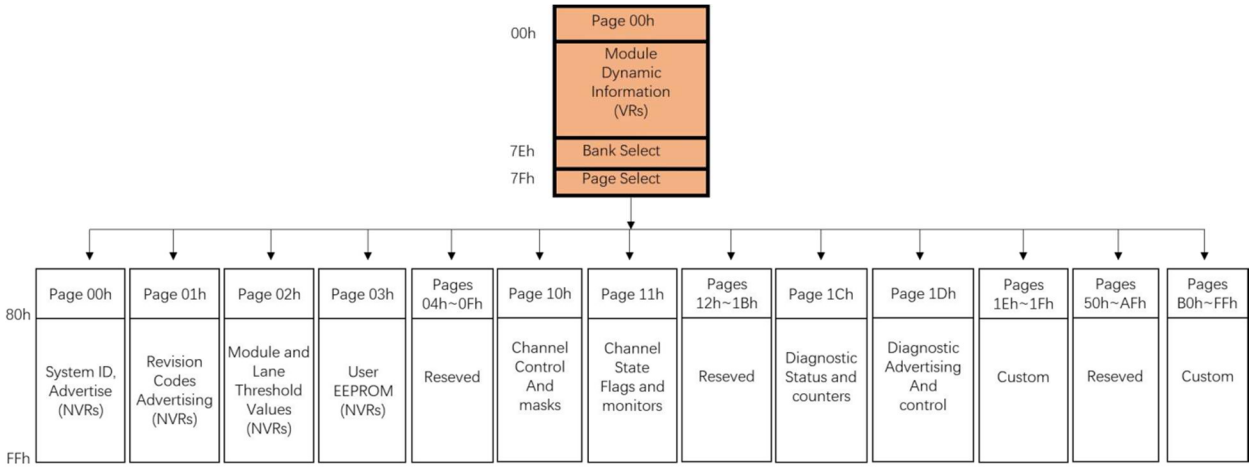
Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Notes:

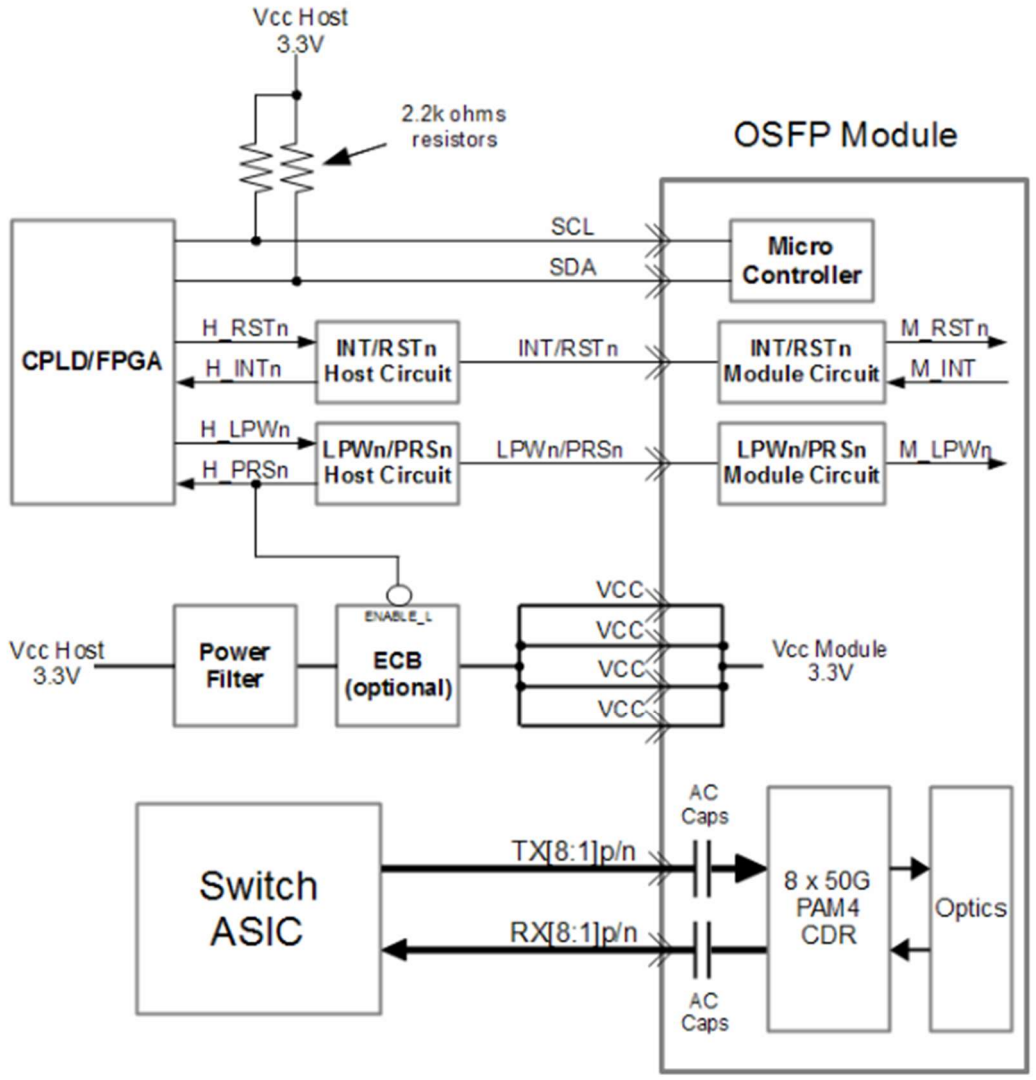
1. OSFP uses common ground (GND)for all signals and supply (power). All are common within the OSFP module and all module voltages are referenced to this potential unless otherwise Noted.
2. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 90 ohms and less than 108
3. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1, 2, 3. Contact sequence 1 will make, then break contact with additional 2, 3 pads.

8. EEPROM Memory Map

CMIS Module Memory Map

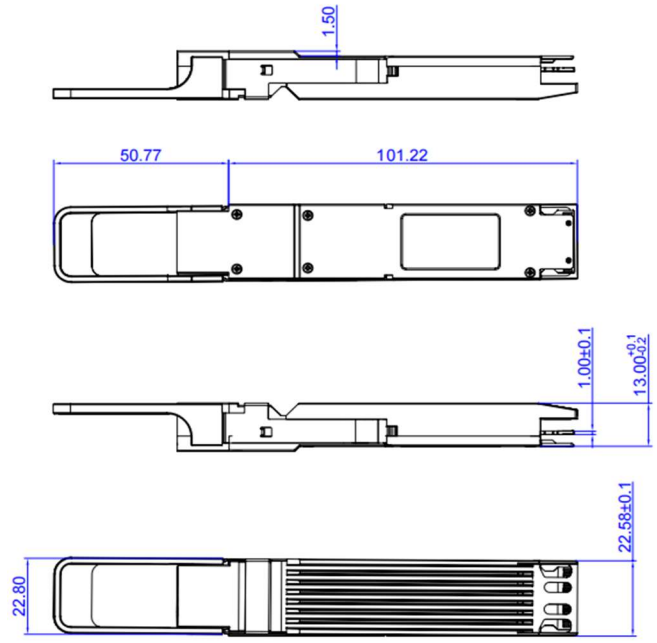


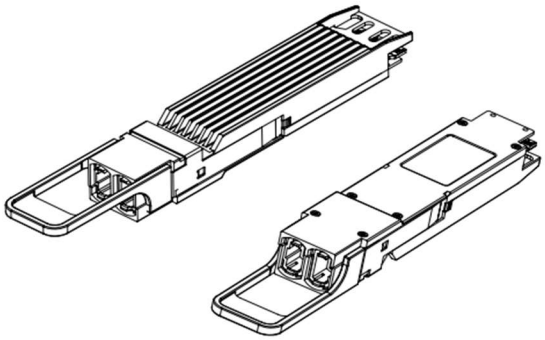
9. Optical Module Block Diagram



10. Mechanical Drawing

Dimensions are in millimeters. (Unit: mm)





11. Ordering information

Part. No	Specifications						
	Pack	Rate (Gbps)	Tx (nm)	Rx	Case Temp (℃)	Reach (m)	Others
MHCG8D5-DNC-8VT1	OSFP	800	1310	PIN	0~+70	500	RoHS