MSLG20-D6C-DT1

Features

- Single fiber bi-directional data links asymmetric TX 2488Mbps/RX1244Mbps application
- 1490nm continuous-mode DFB laser transmitter and 1310nm burst-mode APD-TIA receiver
- Small Form Factor Pluggable package with SC/UPC Connector
- 0 to 70°C operating temperature
- Single 3.3V power supply
- Digital diagnostic monitoring interface
- Digital burst RSSI function to monitor the received optical power level
- LVPECL compatible data input/output interface
- LVTTL transmitter disable control
- LVTTL transmitter laser fault alarm
- Fast LVTTL receiver Signal Detect (SD) indication response
- Low EMI and excellent ESD protection
- Class I laser safety standard IEC-60825 compliant
- RoHS6 Compliance

Applications

- Gigabit-capable Passive Optical Networks (GPON)

Standards

- Complies with SFP Multi-Source Agreement (MSA) SFF-8074i
- Complies with ITU-T G.984.2
- Complies with FCC 47 CFR Part 15, Class B
- Complies with FDA 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated June 24, 2007
- Complies with SFF-8472
- Compatible with TR-NWT-000870 4.1 ESD sensitivity classification Class2.
- Compatible with Telcordia GR-468-CORE

Specification

Absolute Maximum Ratings				
Parameter	**Symbol**	**Min**	**Max**	**Unit**
Storage Ambient Temperature	T_{STG}	-40	85	℃
Storage Humidity	H_S	5	90	%
Operating Humidity	H_O	5	85	%
Power Supply Voltage	V_{CC}	0	+3.6	V

Recommended Operating Conditions					
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
Operating Case Temperature	T_C	0		70	℃
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Supply Current	I_{CC}			500	mA
Power Consumption	P_W			1.65	W
Data Rate			TX 2.488 / RX 1.244		Gbps

Electrical Characteristics						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Transmitter Differential Input Voltage		600		1600	mV	
Receiver Differential Output Voltage		400		1600	mV	LVPECL, DC Coupled
Transmit Fault Alarm Voltage	V_{OH}	2.4		V_{CC}	V	LVTTL
	V_{OL}	0		0.4	V	LVTTL
Transmit Disable Voltage	V_{OH}	2		V_{CC}	V	LVTTL
	V_{OL}	0		0.8	V	LVTTL
Input Differential Impedance		90	100	110	Ω	
Transmit Disable Assert Time	T_{OFF}			100	us	
Signal Detect Voltage	V_{OH}	2.4		V_{CC}	V	LVTTL
	V_{OL}	0		0.4	V	LVTTL
Reset Signal	V_{OH}	2.0		V_{CC}	V	LVTTL
	V_{OL}	0		0.8	V	LVTTL

Optical transmitter Characteristics						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Launched Power (avg.)	P_{OUT}	+6		+10	dBm	
Operating Wavelength Range	λ_C	1480		1500	nm	
Spectral Width (-20dB)	$\Delta\lambda$			1	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Extinction Ratio	ER	8.2			dB	PRBS 2^{23}-1 @2.488Gbit/s
Transmitter and Dispersion Penalty	TDP			1	dB	Transmit on 20km SMF
Optical Output Power after TX Disable	P_{DIS}			-39	dBm	
Output Eye Diagram	Compliant with ITU-T G.984.2					
Transmitter Reflectance Tolerance		-10			dB	
Optical Receiver Characteristics						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Wavelength Range	λ_C	1260		1360	nm	
Receiver Sensitivity	P_{SEN}			-33	dBm	PRBS 2^{23}-1+72CID @1244Mbps, BER<10^{-4} transmitter is operating
Optical Power Input Overload	S_{AT}	-12			dBm	
Dynamic Range		15			dB	Figure 1
Receiver Reflectance				-15	dB	

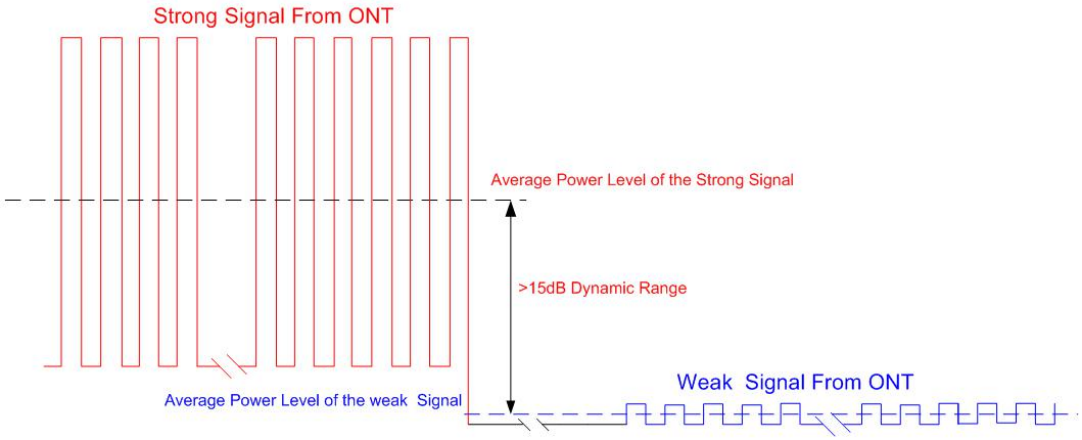

Figure 1 Burst Mode Receiver Dynamic Range in GPON System

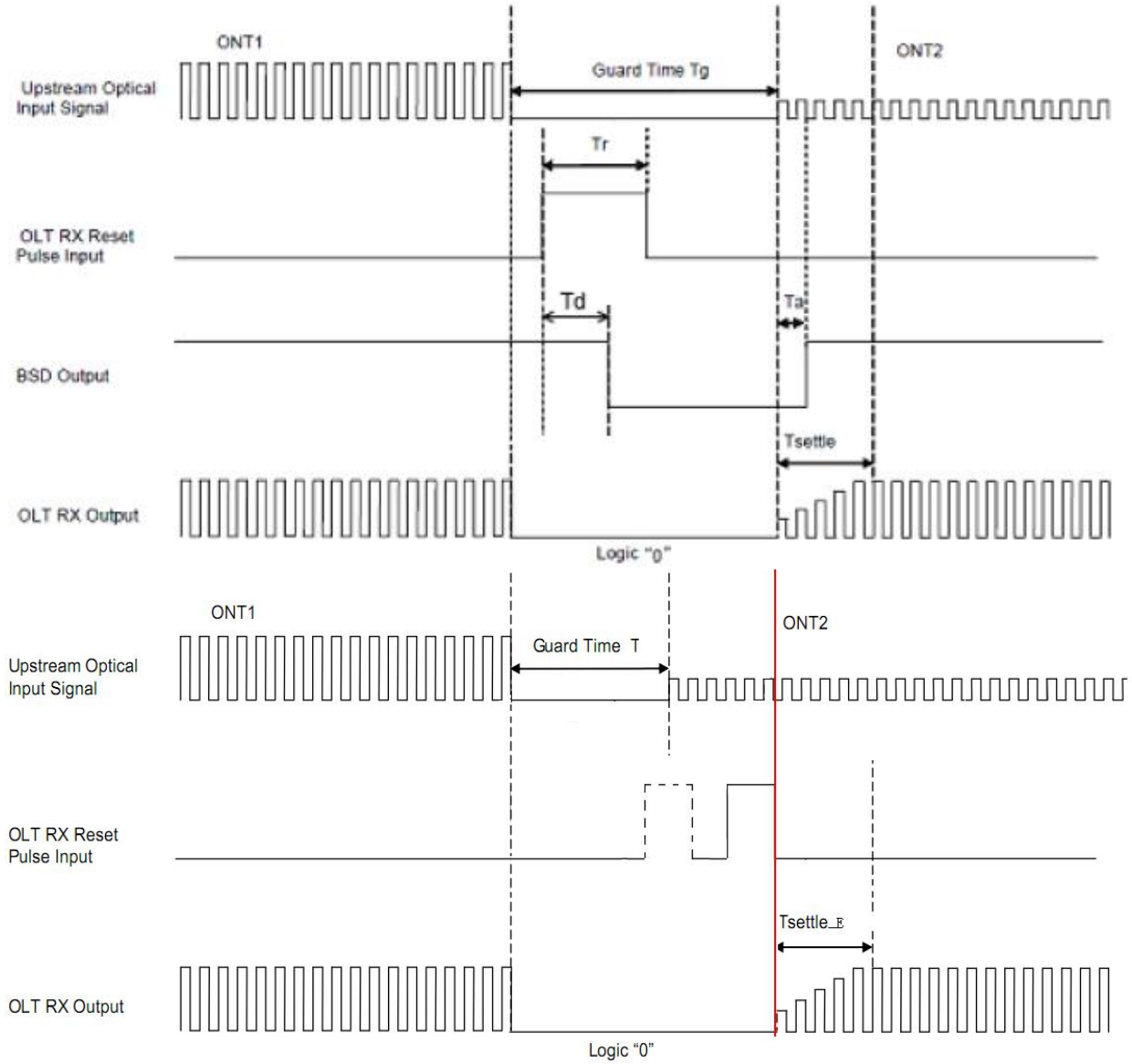

Figure 2 Burst Receiver Timing Sequence

Receiver Timing Characteristics						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Notes**
Guard Time	T_G	32			bit	
Reset Pulse Width(1)	T_R		16		bit	
Receiver Amplitude Recovery Time(2)	T_{SETTLE}			24	bit	
	T_{SETTLE_E}			16	bit	
Signal Detect Assert Time	T_A			25	ns	
Signal Detect De-assert Time	T_D			10	ns	

(1) Reset Pulse support 2 modes in Figure2.

(2) SD signal pulls down immediately after Reset signal, and pulls up while detected RX burst signal till

the next Reset signal.

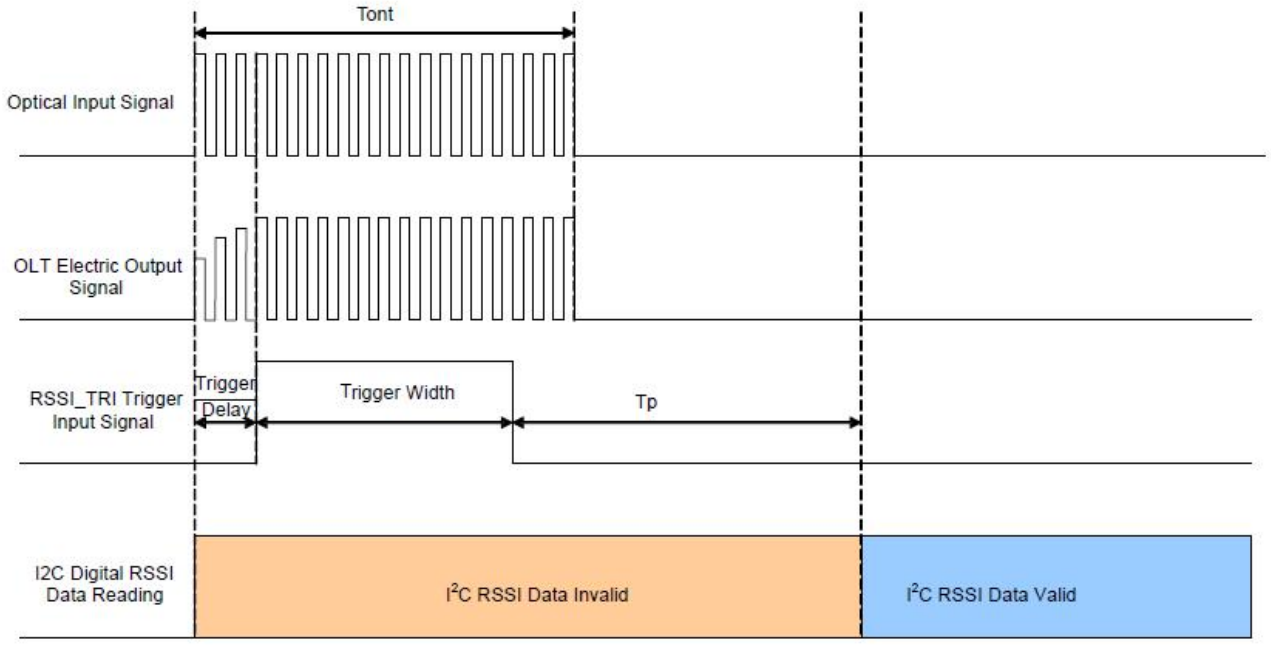

Figure 3 RSSI Timing Sequence

RSSI Characteristics						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Notes**
RSSI Trigger-Low		0		0.8	V	
RSSI Trigger-High		2.0		Vcc	V	
RSSI Trigger Delay	T_D	300		3000	ns	
Optical Signal During Time	T_{ONT}	800			ns	
RSSI Trigger width	T_W		500	T_{ONT} - T_D	ns	
I2C Access Prohibited Time	Tp			500	μs	

Digital Diagnostic Monitoring Information

Parameter	Accuracy	Calibration	Note
Temperature	±3°C	Internal	
Voltage	±3%	Internal	
Bias Current	±10%	Internal	
TX Power	±3dB	Internal	
RX Power	±3dB	Internal	-33 to -12dBm

Note: The digital diagnostic monitoring interface defines 256-byte memory map in EEPROM, which makes use of the 8 bit address 1010001X(A2h). Please refer to the SFF-8472 for the detail information.

Pin definition

Pin No	Symbol	Name/Description	Power Seq.	Note
1	$V_{EE}T$	Transmitter Ground	1st	
2	TX Fault	Transmitter Fault Indication	3rd	High: abnormal; Low: normal
3	TX Disable	Transmitter Disable	3rd	High: transmitter disable; Low: transmitter enable. Internally 4.7k-10kΩ pull-up.
4	MOD-DEF2	Module Definition 2	3rd	The data line of two wire serial interface
5	MOD-DEF1	Module Definition 1	3rd	The clock line of two wire serial interface
6	MOD-DEF0	Module Definition 0	3rd	Connected to Ground in the transceiver
7	Reset	Receiver Reset	3rd	High: reset the receiver
8	SD	Signal Detect	3rd	High: signal is detected; Low: loss of signal;
9	RSSI Trigger	RSSI Trigger for Transceiver A/D Conversion	3rd	High: enable RSSI A/D conversion
10	$V_{EE}R$	Receiver Ground	1st	
11	$V_{EE}R$	Receiver Ground	1st	
12	RD-	Inv. Receiver Data Out	3rd	LVPECL logic output, DC coupled
13	RD+	Receiver Data Out	3rd	LVPECL logic output, DC coupled
14	$V_{EE}R$	Receiver Ground	1st	
15	$V_{CC}R$	Receiver Power	2nd	
16	$V_{CC}T$	Transmitter Power	2nd	
17	$V_{EE}T$	Transmitter Ground	1st	
18	TD+	Transmit Data In	3rd	LVPECL logic input, AC coupled
19	TD-	Inv. Transmit Data In	3rd	LVPECL logic input, AC coupled
20	$V_{EE}T$	Transmitter Ground	1st	

Typical application Circuit

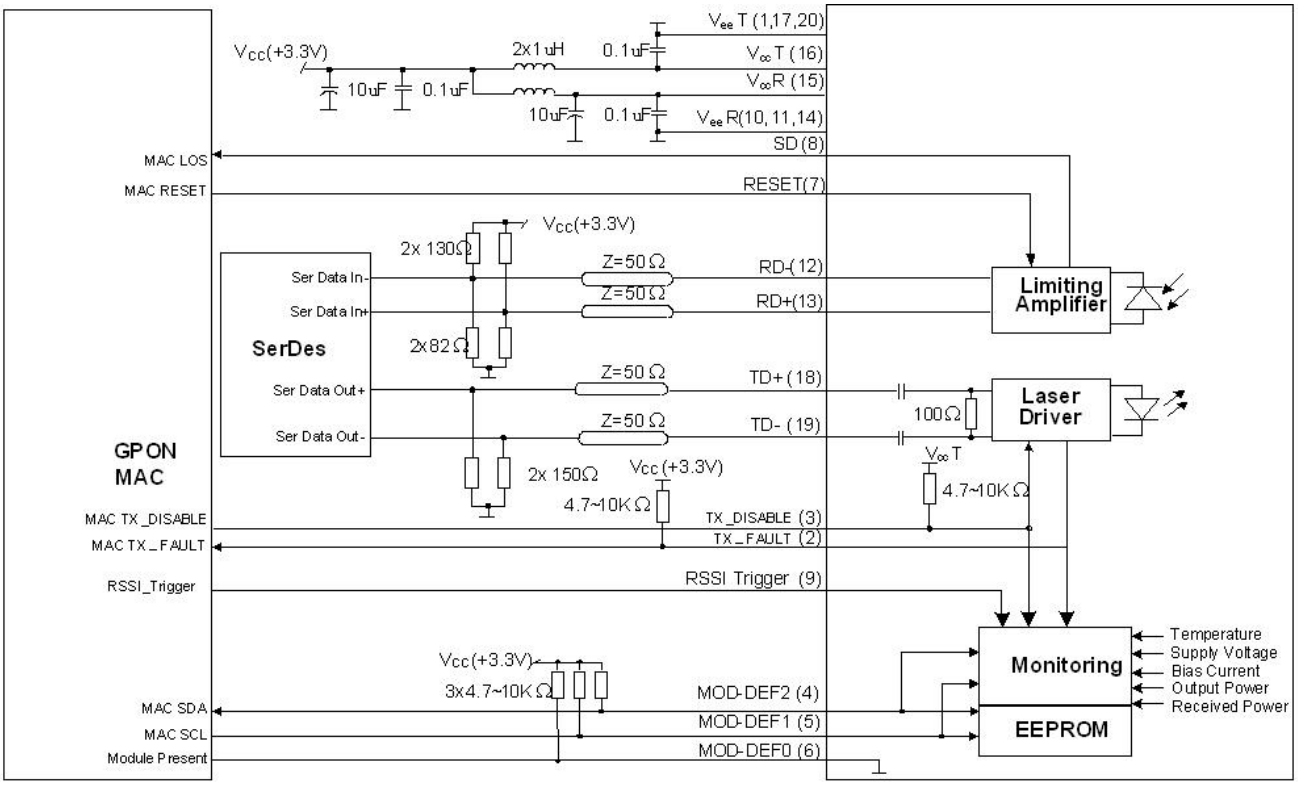

Figure 4 Typical Interface Circuit

EEPROM Memory Map

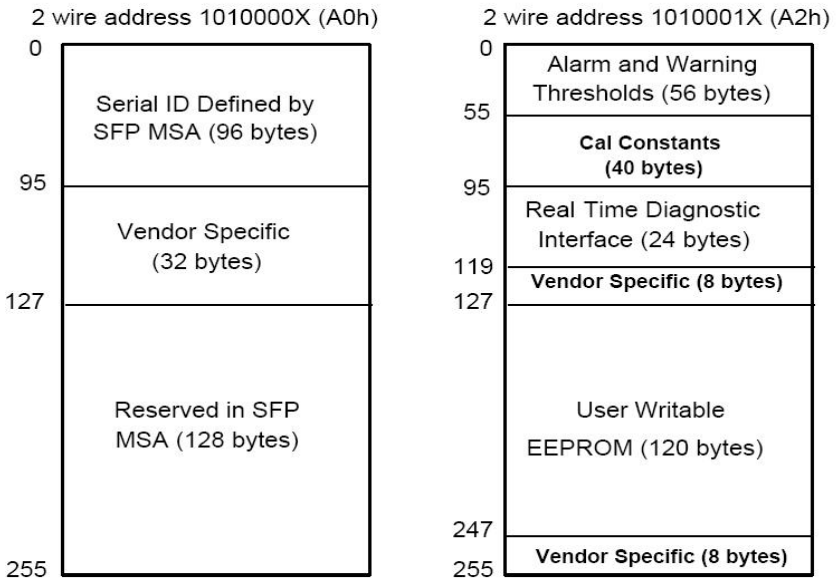

Figure 5 EEPROM Memory Map Specific Data Field Descriptions

EEPROM Serial ID Memory Contents

The optical transceiver contains an EEPROM. It provides access to sophisticated identification information that describes the transceiver's capabilities, standard interfaces, manufacturer, and other information. When the serial protocol is activated, the host generates the serial clock signal (SCL, Mod Def 1). The positive edge clocks data into those segments of the EEPROM that are not writing protected within the SFP transceiver. The negative edge clocks data from the SFP transceiver. The serial data signal (SDA, Mod Def 2) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially.

The Module provides diagnostic information about the present operating conditions. The transceiver generates this diagnostic data by digitization of internal analog signals. Calibration and alarm/warning threshold data is written during device manufacture. Received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring all are implemented. The diagnostic data are raw A/D values and must be converted to real world units using calibration constants stored in EEPROM locations 56 – 95 at wire serial bus address A2h. The digital diagnostic memory map specific data fields define as following.

EEPROM Serial ID Memory Contents (2-Wire Address A0h)

Address	Name of field	Hex	Description
BASE ID Fields			
00	Identifier	03	SFP transceiver
01	Ext. Identifier	04	Serial ID module supported for SFP
02	Connector	01	SC
03-05	Transceiver Codes	00 00 00	Not defined
06	Transceiver Codes	00	Not defined
07-10	Transceiver Codes	00 00 00	Not defined
11	Encoding	03	Encoding codes
12	BR, Nominal	19	
13	Rate Identifier	00	Not defined
14	Length(9um)-km	14	
15	Length(9um)-m	C8	
16	Length(50um)	00	Transceiver transmit distance
17	Length(62.5um)	00	
18	Length(cable)	00	Not support cable

19	Length(OM3)	00	Not support OM3
20-35	Vendor Name	4D 45 4E 54 45 43 48 4F 50 54 4F 20 20 20 20 20	“MENTECHOPTO”(ASCII character)
36	Reserved	00	Not defined
37-39	Vendor OUI	00 00 00	Not defined
40-55	Vendor P/N	4D 53 4C 47 32 30 2D 44 36 43 2D 44 54 31	“MSLG20-D6C-DT1”(ASCII character)
56-59	Vendor P/N Rev.	41 30 20 20	“A0”(ASCII character)
60-61	Laser Wavelength	05 D2	1490nm
62	Reserved	00	Not defined
63	CC_BASE	xx	Check sum of bytes 0-62
Extended ID Fields			
64-65	Options	00 1C	TX_Disable、TX_Fault and RX_SD are implemented
66	BR，max	00	Not specified
67	BR，min	00	Not specified
68-83	Vendor SN	xx…..xx	Vendor Serial Number in ASCII character
84-91	Date Code	Data Code	Vendor Date Code in ASCII character
92	Diagnostic Monitoring Type	68	Digital Diagnostic monitoring implemented “Internal calibrated ” is implemented
93	Enhanced options	E0	Optional Alarm/warning flags, soft Tx_Disable control and monitoring, soft Tx_Fault monitoring are implemented
94	SFF-8472 compliant	08	SFF-8472 compliant with revision 12.0
95	CC-EXT	xx	Check sum of bytes 64-94
Vendor Specific ID Field			
96-127	Vendor Specific	00	Vendor specific EEPROM
128-255	Reserved	00	Reserved for future use

Digital Diagnostic Monitoring Interface：Alarm and Warning Thresholds (2-Wire Address A2h)

Address	Field Size (Byte)	Bits	Name of Field	Description

00~01	2	ALL	Temp High Alarm	MSB at low address, 95°C
02~03	2	ALL	Temp Low Alarm	MSB at low address, -10°C
04~05	2	ALL	Temp High Warning	MSB at low address, 90°C
06~07	2	ALL	Temp Low Warning	MSB at low address, -5°C
08~09	2	ALL	Voltage High Alarm	MSB at low address, 3.6V
10~11	2	ALL	Voltage Low Alarm	MSB at low address, 3.0V
12~13	2	ALL	Voltage High Warning	MSB at low address, 3.5V
14~15	2	ALL	Voltage Low Warning	MSB at low address, 3.1V
16~17	2	ALL	Bias High Alarm	MSB at low address, 90mA
18~19	2	ALL	Bias Low Alarm	MSB at low address, 1mA
20~21	2	ALL	Bias High Warning	MSB at low address, 70mA
22~23	2	ALL	Bias Low Warning	MSB at low address, 2mA
24~25	2	ALL	TX Power High Alarm	MSB at low address, 8.15dBm
26~27	2	ALL	TX Power Low Alarm	MSB at low address, 5dBm
28~29	2	ALL	TX Power High Warning	MSB at low address, 8dBm
30~31	2	ALL	TX Power Low Warning	MSB at low address, 6dBm
32~33	2	ALL	RX Power High Alarm	MSB at low address, -10dBm
34~35	2	ALL	RX Power Low Alarm	MSB at low address, -35dBm
36~37	2	ALL	RX Power High Warning	MSB at low address, -12dBm
38~39	2	ALL	RX Power Low Warning	MSB at low address, -33dBm
40~55	16	ALL	Reserved	Reserved
56~59	4	ALL	Rx_PWR(4)	Single precision floating point calibration data - Rx optical power. Bit7 of byte 56 is MSB. Bit 0 of byte 59 is LSB. For “internally calibrated” devices, Rx_PWR(4) should be set to zero , and useless.
60~63	4	ALL	Rx_PWR(3)	Single precision floating point calibration data - Rx optical power. Bit 7 of byte 60 is MSB. Bit 0 of byte 63 is LSB. For “internally calibrated” devices, Rx_PWR(3) should be set to zero , and useless.
64~67	4	ALL	Rx_PWR(2)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 64 is MSB, bit 0 of byte 67 is LSB. For “internally calibrated” devices, Rx_PWR(2) should be set to zero, and useless.
68~71	4	ALL	Rx_PWR(1)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 68 is MSB, bit 0 of byte 71 is LSB. For “internally calibrated” devices, Rx_PWR(1) should be set to 1 , and useless.
72~75	4	ALL	Rx_PWR(0)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 72 is MSB, bit 0 of byte 75

				is LSB. For “internally calibrated” devices, Rx_PWR(0) should be set to zero , and useless.
76~77	2	ALL	Tx_I(Slope)	Fixed decimal (unsigned) calibration data, laser bias current. Bit 7 of byte 76 is MSB, bit 0 of byte 77 is LSB. For “internally calibrated” devices, Tx_I(Slope) should be set to 1, and useless.
78~79	2	ALL	Tx_I(Offset)	Fixed decimal (signed two’s complement) calibration data, laser bias current. Bit 7 of byte 78 is MSB, bit 0 of byte 79 is LSB. For “internally calibrated” devices, Tx_I(Offset)should be set to zero , and useless.
80~81	2	ALL	Tx_PWR(Slope)	Fixed decimal (unsigned) calibration data, transmitter coupled output power. Bit 7 of byte 80 is MSB, bit 0 of byte 81 is LSB. For “internally calibrated” devices, Tx_PWR(Slope) should be set to 1 , and useless.
82~83	2	ALL	Tx_PWR(Offset)	Fixed decimal (signed two’s complement) calibration data, transmitter coupled output power. Bit 7 of byte 82 is MSB, bit 0 of byte 83 is LSB. For “internally calibrated” devices, Tx_PWR(Offset) should be set to zero , and useless.
84~85	2	ALL	T (Slope)	Fixed decimal (unsigned) calibration data, internal module temperature. Bit 7 of byte 84 is MSB, bit 0 of byte 85 is LSB.For “internally calibrated” devices, T(Slope) should be set to 1, and useless.
86~87	2	ALL	T (Offset)	Fixed decimal (signed two’s complement) calibration data, internal module temperature. Bit 7 of byte 86 is MSB, bit 0 of byte 87 is LSB. For “internally calibrated” devices, T(Offset) should be set to zero, and useless.
88~89	2	ALL	V (Slope)	Fixed decimal (unsigned) calibration data, internal module supply voltage. Bit 7 of byte 88 is MSB, bit 0 of byte 89 is LSB. For “internally calibrated” devices, V(Slope)should be set to 1 , and useless.
90~91	2	ALL	V (Offset)	Fixed decimal (signed two’s complement) calibration data, internal module supply voltage. Bit 7 of byte 90 is MSB. Bit 0 of byte 91 is LSB. For “internally calibrated” devices, V(Offset) should be set to zero, and useless.
92~94	3	ALL	Reserved	Reserved

95	1	ALL	Checksum	Byte 95 contains the low order 8 bits of the sum of bytes 0 – 94.
96	1	ALL	Temperature MSB	Internally measured module temperature.
97	1	ALL	Temperature LSB	
98	1	ALL	Vcc MSB	Internally measured supply voltage in transceiver.
99	1	ALL	Vcc LSB	
100	1	ALL	TX Bias MSB	Internally measured TX Bias Current.
101	1	ALL	TX Bias LSB	
102	1	ALL	TX Power MSB	Measured TX output power.
103	1	ALL	TX Power LSB	
104	1	ALL	RX Power MSB	Measured RX input power.
105	1	ALL	RX Power LSB	
106~109	2	ALL	Reserved	Reserved
110	1	7	TX Disable State	Digital state of the TX Disable Input Pin. Updated within 100ms of change on pin.
		6	Soft TX Disable	Read/write bit that allows software disable of laser. Writing ‘1’ disables laser.
		5	Reserved	Reserved
		4	Reserved	Reserved
		3	Reserved	Reserved
		2	TX Fault	Tx Fail Status: 1=TX Fail; 0=TX Normal
		1	Reserved	Reserved
		0	Reserved	Reserved
111	1	ALL	Reserved	Reserved
112	1	7	Temp High Alarm	Set when internal temperature exceeds high alarm level.
		6	Temp Low Alarm	Set when internal temperature is below low alarm level.
		5	Vcc High Alarm	Set when internal supply voltage exceeds high alarm level.
		4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level.
		3	TX Bias High Alarm	Set when TX Bias current exceeds high alarm level.
		2	TX Bias Low Alarm	Set when TX Bias current is below low alarm level.
		1	TX Power High Alarm	Set when TX output power exceeds high alarm level.
		0	TX Power Low Alarm	Set when TX output power is below low alarm level.
113	1	7	RX Power High Alarm	Set when Received Power exceeds high alarm level.
		6	RX Power Low Alarm	Set when Received Power is below low alarm level.

		5	Reserved	Reserved
		4	Reserved	Reserved
		3	Reserved	Reserved
		2	Reserved	Reserved
		1	Reserved	Reserved
		0	Reserved	Reserved
114	1	ALL	Reserved	Reserved
115	1	ALL	Reserved	Reserved
116	1	7	Temp High Warning	Set when internal temperature exceeds high warning level.
		6	Temp Low Warning	Set when internal temperature is below low warning level.
		5	Vcc High Warning	Set when internal supply voltage exceeds high warning level.
		4	Vcc Low Warning	Set when internal supply voltage is below low warning level.
		3	TX Bias High Warning	Set when TX Bias current exceeds high warning level.
		2	TX Bias Low Warning	Set when TX Bias current is below low warning level.
		1	TX Power High Warning	Set when TX output power exceeds high warning level.
		0	TX Power Low Warning	Set when TX output power is below low warning level.
117	1	7	RX Power High Warning	Set when Received Power exceeds high warning level.
		6	RX Power Low Warning	Set when Received Power is below low warning level.
		5	Reserved	Reserved
		4	Reserved	Reserved
		3	Reserved	Reserved
		2	Reserved	Reserved
		1	Reserved	Reserved
		0	Reserved	Reserved
118	1	ALL	Reserved	Reserved
119	1	ALL	Reserved	Reserved
120-127	8	ALL	Vendor Specific	Vendor Specific
128-247	120	ALL	User EEPROM	User writable EEPROM
248-255	8	ALL	Vendor Specific	Vendor Specific

Product Security requirements

Items	Contents
Virus scanning	Don't contain malicious code or code vulnerabilities such as Trojans, viruses, worms, backdoors, etc.
Source code static scanning	Don't contain dead pointers, divide by 0, integer overflow, invalid shift operations, memory management, null pointer indirect references, boundary overflow checks, uninitialized variables, write constants, etc.
Source code security scanning	Don't contain memory leaks, out of bounds errors, arithmetic errors, suspicious code, logic errors, etc.

Package Outline

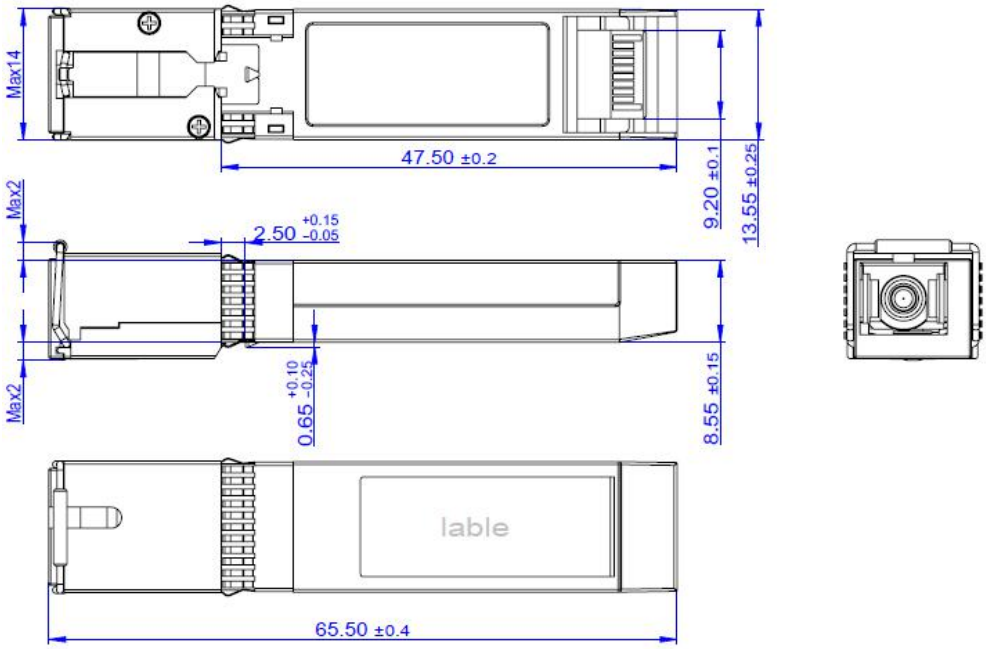

Figure 6 Package Outline

Ordering information

PART NO.	Specifications									
	Package	Type	Rate (Gbps)	Tx (nm)	Po (dBm)	Rx (nm)	Sen (dBm)	Temp (℃)	Reach (km)	DDM
MSLG20-D6C-DT1	SFP	GPON OLT Class C++	2.488 TX/ 1.244 RX	1490	6~10	1310	<-33	0~70	20	Y